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Mail Stop Appeal Brief-Patents

In re application of: Kraig R. WHITE

Attorney Docket No. FIS920010178US1

Application No. : 10/066,497

Group Art Unit : 2133

Filed : February 1, 2002

Examiner : Joseph D. Torres

For : CHECK BIT FREE ERROR CORRECTION FOR SLEEP MODE DATA RETENTION

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Transmitted herewith is an ~~Appeal Brief~~ **under 37 C.F.R. 41.37** in the above-captioned application.

____ Small Entity Status of this application under 37 C.F.R. 1.9 and 1.27 has been established by a previously filed statement.

____ A verified statement to establish small entity status under 37 C.F.R. 1.9 and 1.27 is enclosed.

____ A Request for Extension of Time.

____ No additional fee is required.

The fee has been calculated as shown below:

Claims After Amendment	No. Claims Previously Paid For	Present Extra	Small Entity		Other Than A Small Entity	
			Rate	Fee	Rate	Fee
Total Claims: 20	*20	0	x25=	$	x 50=	$ 0.00
Indep. Claims: 3	**3	0	x100=	$	x200=	$ 0.00
Extension Fees for ____ Month(s)				$		$ 0.00
Appeal Brief Filing Fee				$		$500.00
			Total:	$	Total:	$500.00

* If less than 20, write 20
** If less than 3, write 3

__X__ Please charge my Deposit Account No. 09-0458 (Fishkill) in the amount of $500.00.

N/A A check in the amount of $_____ to cover the filing/extension fee is included.

__X__ The U.S. Patent and Trademark Office is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 09-0458 (Fishkill).

__X__ Any additional filing fees required under 37 C.F.R. 1.16.

__X__ Any patent application processing fees under 37 C.F.R. 1.17, including any required extension of time fees in any concurrent or future reply requiring a petition for extension of time for its timely submission (37 C.F.R. 1.136(a)(3)).

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P27182.A04
Docket No.: FIS920010178US

Customer No.: 45988

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant : Kraig R. WHITE

Confirmation No.: 4513

Appln. No. : 10/066,497

Group Art No.: 2133

Filed : August 5, 1998

Examiner: J. Torres

For : CHECK BIT FREE ERROR CORRECTION FOR SLEEP MODE DATA CORRECTION

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

This appeal is from the Examiner's final rejection of claims 1 - 20 as set forth in the Final Office Action of November 16, 2004.

A Notice of Appeal in response to the November 16, 2004 Final Office Action was filed April 14, 2005. Further, the instant Appeal Brief is being timely submitted by the initial due date of June 14, 2005.

Appellant authorizes the charging of the requisite fee under 37 C.F.R. 41.20 (b)(2) in the amount of $ 500.00 for the filing of the Appeal Brief, as well as any other fees necessary to ensure consideration of the instant Appeal Brief, to **IBM Deposit Account No. 09 – 0458** (Fishkill).

(1) REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, Armonk, New York 10504 as evidenced by the Notice of Recordation dated February 1, 2002 at Reel 012574 and Frame 0163.

(2) RELATED APPEALS AND INTERFERENCES

No related appeals and/or interferences are pending.

(3) STATUS OF THE CLAIMS

Claims 1 - 20, the only claims pending in the instant application, stand finally rejected.

(4) STATUS OF THE AMENDMENTS

No amendments have been entered subsequent to the Final Office Action of November 16, 2004. However, the Examiner has not yet indicated whether Appellant's Amendment Under 37 C.F.R. 1.116 filed March 4, 2005 will be entered for the purpose of the instant appeal.

An Amendment Under 37 C.F.R. 1.116 was filed on January 18, 2005, which included amendments to claims 1 and 8 to address formal matters. Moreover, the amendment included an in advertent change to claim 10. In the Advisory Action of February 25, 2005, the Examiner refused entry of the amendment because the inadvertent change to claim 10 raised new issues.

In reply, Appellant submitted an Amendment Under 37 C.F.R. 1.116 on March 4, 2005, which included the amendments to claims 1 and 8, and which addressed the inadvertent change to claim 10. To date, the Examiner has not answered this amendment.

Accordingly, Appellant notes that Section 8 of the instant Appeal Brief, i.e., Claims Appendix, includes a Part I that includes claims 1 and 8 in their forms assuming the Amendment Under 37 C.F.R. 1.116 filed March 4, 2005 is not entered by the Examiner for the purpose of the instant appeal, and a Part II that includes claims 1 and 8 in their amended forms assuming the Amendment Under 37 C.F.R. 1.116 filed March 4, 2005 is entered for the purpose of the pending appeal.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The instant invention is directed to semiconductor dynamic random access memories (DRAMs) and, more particularly, to correcting bit errors arising during sleep mode due to a reduced DRAM refresh rate. (Specification Page 1, lines 10 – 13). In particular, an exemplary embodiment of the invention is directed to a memory system, such as a DRAM, having a reduced refresh rate in a sleep mode to conserve power wherein ECC encoding occurs at the time of entering the sleep mode. ECC decoding for error detection and correction need only take place upon wake up when resuming active mode. In addition, the memory system reassigns a portion of the memory for storing the additional parity bits required for the error correcting code (ECC). In operation, when the memory system enters sleep mode DRAM addresses storing non-critical bits in the DRAM are identified. These addresses are reassigned as a second memory space designated for storing ECC parity bits. The ECC encoding circuit encodes critical data bits with an additional error correcting parity bits which are stored in the second memory space designated for storing ECC parity bits. The ECC is chosen having the capability to correct a predetermined number of bit errors. A variable rate refresh circuit decreases the DRAM refresh rate to a point where the statistical number of errors that would arise due to the reduced refresh rate does not exceed the correction capability of the ECC used. Upon exiting sleep mode an ECC decoding circuit decodes the encoded data and corrects any detected errors to the critical data. Thereafter, the ECC parity bits are discarded and the second memory space is released and becomes available for normal operations. (Specification Page 5, lines 3 – 27).

The following descriptions are made with respect to the independent claims and include references to particular parts of the specification. As such, the following are merely exemplary and are not a surrender of other aspects of the present invention that are also enabled by the present specification and that are directed to equivalent structures or methods within the scope of the claims.

Independent claim 1 is directed to a memory system having a reduced refresh rate in a sleep mode includes a dynamic memory 13, (specification page 6, line 21; and Figure 1), an error correction code (ECC) memory allocation circuit 12 for identifying non-critical bit addresses in the dynamic memory and allocating the addresses as ECC addresses when entering from an active mode to sleep mode, and an ECC encoder 3 for encoding critical bits with error correction codes. The error correction codes are stored in the ECC addresses. (Specification page 7, lines 13 – 29;

and Figure 1). A refresh execution circuit 15 for reducing a refresh rate in the sleep mode and increasing the refresh rate in the active mode, (specification page 8, lines 8 – 10; and Figure 1), and an ECC decoder 5 for decoding the critical bits encoded with the error correction codes when reentering the active mode. (specification page 8, lines 16 – 19; and Figure 1).

Independent claim 10 is directed to a method for reducing the refresh rate of a memory in sleep mode, that includes switching from an active mode to a sleep mode 32, identifying non-critical bit addresses 34, encoding critical bits with an error correction code (ECC) 36, storing ECC codes at said non-critical bit addresses 38, reducing a refresh rate for said memory40, performing error correction on said critical bits using said ECC codes when reentering active mode 42, anddiscarding said ECC bits 44. (Specification page 9, line 30 – page 11, line 8; and Figure 3).

Independent claim 15 is directed to a computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode, including switching from an active mode to a sleep mode 32, identifying non-critical bit addresses 34, encoding critical bits with an error correction code (ECC) 36, storing ECC codes in said non-critical bit addresses 38, reducing a refresh rate for said memory 40, performing error correction on said critical bits using said ECC codes when reentering active mode 42, and discarding said ECC bits 44. (Specification page 9, line 30 – page 11, line 8; and Figure 3).

(6) **GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

(A) Claims 1 – 9 are Rejected Under 35 U.S.C. § 112, second paragraph, as being indefinite;

(B) Claims 1 – 5, 7 – 11, 13, and 14 are Rejected Under 35 U.S.C. § 102(b) as Anticipated by ITO et al. (U.S. Patent No. 6,697,992) [hereinafter "ITO"]; and

(C) Claims 6, 12, and 15 – 20 are Rejected Under 35 U.S.C. § 103(a) as Unpatentable Over ITO.

(7) **ARGUMENT**

(A) The Rejection of Claims 1 – 9 Under 35 U.S.C. § 112, Second Paragraph, as being Indefinite is in Error, the Rejection Should be Reversed, and the Application Should be Remanded to the Examiner.

Claims 1 and 8 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regard as the invention.

As noted above, as of the filing of the instant Appeal Brief, the Examiner has not indicated whether the Amendment Under 37 C.F.R. 1.116 filed March 4, 2005 will be entered for the purpose of the pending appeal. For the purpose of addressing this formal rejection on appeal, Appellant submits that entry of the above-identified Amendment Under 37 C.F.R. 1.116 will render moot the instant formal rejection, and that entry of the amendment is proper in that it does not raise any no new issues for consideration by Examiner nor any question of new matter.

In particular, the term "said refresh rate" in lines 12-14 of independent claim 1 has been amended to "a refresh rate," in order to provide proper antecedent basis. Accordingly, Appellant submits that no new issues are raised for consideration by the Examiner nor is any question of new matter raised, such that entry of the amendment will render moot the formal rejection of independent claim 1.

Further, claim 8 has been amended to recite:

> wherein said ECC memory allocation circuit reassigns said non-critical bit addresses as a second memory space designated for storing ECC parity bits.

Appellant respectfully submits that claim 8, as amended, is clear and unambiguous, and that the amendment clarifies the claim terminology without raising any new issues for consideration by the Examiner and without raising any question of new matter. Thus, Appellant submits that entry of the instant amendment will likewise render the formal rejection of claim 8 under § 112, second paragraph, moot.

Accordingly, Appellant requests that the Board reverse the Examiner's decision to finally reject claims 1 – 9 based upon formal matters, and remand the application to the examining group for early allowance.

(B) The Rejection of Claims 1 – 5, 7 – 11, 13, and 14 Under 35 U.S.C. § 102(b) As

Anticipated by ITO is in Error, the Rejection Should be Reversed, and the Application Should be Remanded to the Examiner.

The Examiner asserts that ITO shows a memory system having a reduced refresh rate in a sleep mode that includes the recited features of the pending claims. Moreover, the Examiner asserts that Exhibit A, submitted with Appellants' September 9, 2004 Declaration Under 37 C.F.R. 1.131, fails to show, for the purpose of reduction to practice, the recited feature of a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode, as recited in independent claim 1. Appellant traverses the Examiner's assertions.

Appellant initially notes that the Examiner has objected to the Declaration Under 37 C.F.R. 1.131 based upon an asserted failure to show a feature recited in independent claim 1. However, Appellant submit that, as the Examiner has not pointed to or asserted any defect in the 131 Declaration with regard to independent claims 10 and 15, it is understood that, for the purposes of claims 10 – 20, the 131 Declaration is acceptable in removing ITO as prior art against the subject matter of claims 10 – 20. Accordingly, Appellant submits that the rejection of claims 10, 11, 13, and 14 is moot, and respectfully requests that the Board reverse the rejection with regard to these claims, and remand the application to the examining group for early allowance of claims 10, 11, 13, and 14.

Because the Examiner has not yet replied to Appellant's Amendment Under 37 C.F.R. 1.116 filed March 4, 2005, Appellant is not certain whether the Examiner's rejection is based solely upon the formal rejection in independent claim 1. Assuming that the Examiner's asserted defect of Appellant's 131 Declaration is merely based upon the formal matter noted in independent claim 1, i.e., the term "said refresh rate," Appellant submits that the asserted defect would be rendered moot by entry of Appellant's March 4, 2005 Amendment Under 37 C.F.R. 1.116.

Moreover, Appellant submits that the Rule 131 Declaration is formally and substantively sufficient to establish that the inventor had conceived and reduced to practice with due diligence the invention defined in at least independent claims 1, 10, and 15 starting before the effective date of the primary reference to ITO, *i.e.*, August 8, 2001.

Assuming that the Examiner's assertions are based upon a belief that the recited feature of independent claim 1, notwithstanding formal matters, is not shown in the Exhibit A filed with the 131 Declaration, Appellant requests that the Board reverse the Examiner's decision to finally

reject the claims. One ordinarily skilled in the DRAM art at the time the invention was made would understand Exhibit A as disclosing a refresh execution circuit for reducing the refresh rate during sleep mode, and increasing the refresh rate in active mode.

As shown in Exhibit A, one of the features of developing low power DRAMS is a longer cell retention time to facilitate a slower refresh frequency in the end product application. This reduces the power associated with refreshing the DRAM. More specifically, under the heading "Projected Benefit," Exhibit A discloses a reduced refresh rate in sleep mode and an increased refresh rate in active mode, i.e., there is a longer sleep mode (SM) retention time as shown in the example of 80 ms at 85°C and 600 ms at 40°C. Accordingly, Appellant submits that Exhibit A shows a reduced refresh rate in the sleep mode.

Further, a person of ordinary skill in the DRAM art reviewing Exhibit A would understand the refresh rate is increased in active mode. Specifically, Exhibit A discloses:

> Upon exiting SM, ECC is used to correct any retention time fails that occurred during sleep; ECC bits are discarded and the *total DRAM becomes available* for end application utilization (emphasis added).

Thus, Appellant submits that Exhibit A provides an increased refresh rate upon exiting sleep (SM). Normal operation of a DRAM requires that the DRAM be refreshed at a rate that satisfies the worst case retention time (80 ms as indicated on page 2 of the Office Action) for the cells in the DRAM over the whole operating temperature for the junction temperature of the device.

Thus, Exhibit A demonstrates that the inventor, at the time of the invention, from conception to reduction to practice, recognized the elements set forth in claims 1, 10, and 15. Accordingly, Appellant submits the Declaration Under 37 C.F.R. 1.131 and the accompanying documents were sufficient to overcome the §102(e) rejection.

In addition to providing sufficient disclosure of the subject matter purportedly disclosed by ITO, the statements in the Declaration show that the formal requirements of §1.131 are satisfied, namely:

(1) the rejections to be overcome are under §102(e) and §103(a);
(2) all the acts for completing the invention of claims 1, 10 and 15 were performed in this country, and
(3) the effective date of the Ito reference, i.e., August 8, 2001, is not more than one year prior to the filing date of the present application in this country.

It is respectfully submitted that the statements in the Declaration are sufficient to satisfy the substantive requirements of 37 C.F.R. §1.131. The Declaration sets forth specific facts, of sufficient character and weight, to establish a **date of conception** before the effective date of the ITO reference of August 8, 2001, and to show that the Inventor and his attorneys exercised **due diligence** from a time before the effective filing date of the ITO reference to a constructive reduction to practice, i.e., to the filing of the application.

Date of Conception

As stated in the Declaration, a memory system having a reduced refresh rate in a sleep mode, and a method for reducing the refresh rate of a memory in sleep mode, as disclosed and recited in claims 1, 10, and 15 of the application (and those claims dependent thereon) was conceived by the Inventor before the effective date of the Ito reference. Invention disclosure documentation is submitted with the Declaration as supporting evidence of this prior date of conception. It is respectfully submitted that at least the invention disclosure evidence shows that the Inventor had a definite and permanent idea of the complete and operative invention of claims 1, 10, and 15, as presently pending, prior to the August 8, 2001 effective date of the Ito reference.

In particular, the accompanying evidence shows, textually and pictorially, the features of claims 1, 10, and 15. The original copy of the invention disclosure documentation evidences a date antedating the August 8, 2001 effective date of the ITO reference. This and all other pertinent dates have been removed from the photocopies submitted with the Declaration to prevent any potential prejudice to Appellant. It is noted that the figures provided are illustrative in nature and are not intended as limiting features of the invention.

Appellant further submits that the Declaration shows, unequivocally, that the Inventor had in their possession a definite and permanent idea of the complete and operative invention of claims 1, 10, and 15 starting before August 8, 2001 in a manner sufficient to satisfy the requirements of conception, as set forth in M.P.E.P. §§ 715.07 and 2138.04, and thus constitute *prima facie* evidence of Appellant's date of conception of the invention in this country before the effective date of the Ito reference.

Due Diligence

Appellant further submits that the Declaration shows the Inventor and his attorneys exercised due diligence from a time before the August 8, 2001 effective date of the ITO reference

to a constructive reduction to practice, realized by the filing of the above-identified patent application on February 1, 2002.

The invention disclosure documentation was completed by the Inventor prior to the ITO reference date of August 8, 2001. IBM authorized outside counsel at the undersigned firm to prepare the application, and supplied the invention disclosure to outside counsel in a timely manner. Numerous discussions between the Inventor and counsel took place until a first draft of the application was forwarded to Inventor, Kraig R. White. Revisions were made and subsequent drafts were prepared and reviewed by the Inventor, until a final draft was forwarded to IBM for execution on January 12, 2002, and subsequent filing on February 1, 2002.

Outside patent counsel also acted in an expeditious manner to prepare and forward the application to filing. Under M.P.E.P. § 2138.06, only ***reasonable*** diligence is required in this regard. More specifically, § 2138.06 states that a patent attorney will be held to have exercised reasonable diligence if the attorney worked reasonably hard on the application during the critical period, taking into consideration any backlog of unrelated cases the attorney may have had and his completion of those cases along with the present application in chronological order.

Appellant's Declaration avers that his patent attorneys acted sufficiently expeditiously to satisfy the requirements of due diligence. Appellant submits that the Declaration submitted herewith are sufficient to show that the Inventor and his attorneys exercised the due diligence required under 37 C.F.R. § 1.131. The Declaration shows that the Inventor remained in regular contact with patent attorneys to answer questions, provide technical explanation, and supply the supplemental disclosure materials necessary for enabling the application to be filed in an expeditious manner.

As Exhibit A discloses all of the subject matter purportedly disclosed in ITO and as all the formal requirements of Rule 131 have been complied with, Appellant submits that the rejections of claims 1 – 5, 7 – 11, 13, and 14 are rendered moot in view of the Declaration Under 37 C.F.R. §1.131 filed September 9, 2004. More specifically, Appellant submits that the Rule 131 Declaration is formally and substantively sufficient to establish that the inventor had conceived and reduced to practice with due diligence the invention defined in at least independent claims 1, 10, and 15 starting before the effective date of the primary reference to ITO, i.e., August 8, 2001.

Accordingly, Appellants respectfully request that the decision of the Examiner to finally reject claims 1 – 5, 7 – 11, 13, and 14 under 35 U.S.C. § 102(b) be reversed, and that the

application be remanded to the Examiner for withdrawal of the rejection over ITO and an early allowance of all claims on appeal.

(C) The Rejection of Claims 6, 12, and 15 – 20 Under 35 U.S.C. § 103(a) Over ITO is in Error, the Rejection Should be Reversed, and the Application Should be Remanded to the Examiner.

As discussed above, as the Examiner has not pointed to or asserted any defect in the Rule 131 Declaration with regard to independent claims 10 and 15, it is understood that, for the purposes of claims 10 – 20, the 131 Declaration is acceptable in removing ITO as prior art against the subject matter of claims 10 – 20. Accordingly, Appellant submits that the instant rejection of claims 12 and 15 – 20 is moot, and respectfully requests that the Board reverse the rejection with regard to these claims, and remand the application to the examining group for early allowance of claims 12 and 15 - 20.

Moreover, Appellant has shown that, as Exhibit A discloses all of the subject matter purportedly disclosed in ITO and as all the formal requirements of Rule 131 have been complied with, the pending rejections are rendered moot in view of the Declaration Under 37 C.F.R. §1.131 filed September 9, 2004. In particular, Appellant submits that the Rule 131 Declaration is formally and substantively sufficient to establish that the inventor had conceived and reduced to practice with due diligence the invention defined in at least independent claims 1, 10, and 15 starting before the effective date of the primary reference to ITO, i.e., August 8, 2001.

Thus, as claims 6, 12, and 16 – 20 depend from independent claims 1, 10, or 15, these claims are allowable at least for the reason that they depend from allowable claims and because they recite subject matter that further defines the invention. Therefore, Appellant submits that the instant rejection is moot.

Accordingly, Appellant respectfully requests that the decision of the Examiner to finally reject claims 6, 12, and 15 – 20 under 35 U.S.C. § 103(a) be reversed, and that the application be remanded to the Examiner for withdrawal of the rejection over the art of record fails to teach or suggest and an early allowance of all claims on appeal.

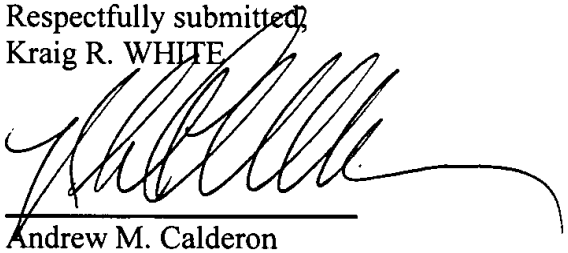
(D) Conclusion

Claims 1 – 9 are fully in compliance with the requirements of 35 U.S.C. § 112, second paragraph; Claims 1 – 5, 7 – 11, 13, and 14 are patentable under 35 U.S.C. § 102(b) over ITO; and Claims 6, 12, and 15 – 20 are patentable under 35 U.S.C. § 103(a) over ITO. Specifically, the

applied art is not prior art against the pending claims, such that ITO cannot anticipate or render unpatentable the unique combination of features recited in Appellant's claims 1 – 20. Accordingly, Appellant respectfully requests that the Board reverse the Examiner's decision to finally reject claims 1 – 9 under 35 U.S.C. §112, second paragraph, claims 1 – 5, 7 – 11, 13, and 14 under 35 U.S.C. § 102(b), and claims 6, 12, and 15 – 20 under 35 U.S.C. § 103(a) and remand the application to the Examiner for withdrawal of the rejection.

Thus, Appellant respectfully submits that each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. §112, second paragraph, 35 U.S.C. §102(b), and 35 U.S.C. § 103(a), and that the present application and each pending claim are allowable over the prior art of record.

Respectfully submitted,
Kraig R. WHITE



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Attachments: Claims Appendix
Evidence Appendix
Related Proceedings Appendix

(8) CLAIMS APPENDIX

Part I – Claims Pending with Amendment Under 37 C.F.R. 1.116 Unentered

1. (Original) A memory system having a reduced refresh rate in a sleep mode, comprising:

a dynamic memory;

an error correction code (ECC) memory allocation circuit for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode;

an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses;

a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode; and

an ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode.

2. (Original) A memory system as recited in claim 1 further comprising a storage device for storing sleep mode refresh rate data.

3. (Original) A memory storage device as recited in claim 2 wherein said storage device comprises a fusible link.

4. (Original) A memory system as recited in claim 1 further comprising:

a storage device for storing a plurality of sleep mode refresh rate data; and

a temperature sensor, wherein said refresh execution circuit selects one of said sleep mode refresh rate data according to operating temperature.

5. (Original) A memory system as recited in claim 4 wherein said storage device comprises a fusible link.

6. (Original) A memory system as recited in claim 4 wherein said refresh rate is reduced by a 2X factor for each decade Celsius reduction in operating temperature.

7. (Previously presented) A memory system as recited in claim 1 wherein said error correction codes comprise one of Reed-Solomon code and Bose-Chaudhuri-Hocquenghem code.

8. (Previously presented) A memory system as recited in claim 1 wherein said ECC memory allocation circuit stores preallocated addresses in said dynamic memory.

9. (Original) A memory system as recited in claim 1 wherein said ECC memory allocation

assigns ECC addresses dynamically to the last byte of each word address.

10. (Original) A method for reducing the refresh rate of a memory in sleep mode, comprising the steps of:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes at said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

11. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the steps of:

determining an operating temperature for said memory; and

selecting one of a plurality of refresh rates based on said operating temperature of said memory.

12. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 11 further comprising the step of:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

13. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the step of:

preallocating addresses in memory to store non-critical bits.

14. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the step of:

storing said ECC codes for a word of a last byte address for said word.

15. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode, the steps comprising:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes in said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

16. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

17. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

preallocating addresses in memory to store non-critical bits.

18. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

storing said ECC codes for a word of a last byte address for said word.

19. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15 wherein said error correction codes comprise Reed-Solomon code.

20. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, wherein said error correction codes comprise Bose-Chaudhuri-Hocquenghem code.

Part II – Claims Pending with Amendment Under 37 C.F.R. 1.116 Entered

1. (Previously presented) A memory system having a reduced refresh rate in a sleep mode, comprising:

a dynamic memory;

an error correction code (ECC) memory allocation circuit for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode;

an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses;

a refresh execution circuit for reducing a refresh rate in said sleep mode and increasing said refresh rate in said active mode; and

an ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode.

2. (Original) A memory system as recited in claim 1 further comprising a storage device for storing sleep mode refresh rate data.

3. (Original) A memory storage device as recited in claim 2 wherein said storage device comprises a fusible link.

4. (Original) A memory system as recited in claim 1 further comprising:

a storage device for storing a plurality of sleep mode refresh rate data; and

a temperature sensor, wherein said refresh execution circuit selects one of said sleep mode refresh rate data according to operating temperature.

5. (Original) A memory system as recited in claim 4 wherein said storage device comprises a fusible link.

6. (Original) A memory system as recited in claim 4 wherein said refresh rate is reduced by a 2X factor for each decade Celsius reduction in operating temperature.

7. (Previously Presented) A memory system as recited in claim 1 wherein said error correction codes comprise one of Reed-Solomon code and Bose-Chaudhuri-Hocquenghem code.

8. (Previously presented) A memory system as recited in claim 1 wherein said ECC memory allocation circuit reassigns said non-critical bit addresses as a second memory space designated for storing ECC parity bits.

9. (Original) A memory system as recited in claim 1 wherein said ECC memory allocation

assigns ECC addresses dynamically to the last byte of each word address.

10. (Original) A method for reducing the refresh rate of a memory in sleep mode, comprising the steps of:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes at said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

11. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the steps of:

determining an operating temperature for said memory; and

selecting one of a plurality of refresh rates based on said operating temperature of said memory.

12. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 11 further comprising the step of:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

13. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the step of:

preallocating addresses in memory to store non-critical bits.

14. (Original) A method for reducing the refresh rate of a memory in sleep mode as recited in claim 10 further comprising the step of:

storing said ECC codes for a word of a last byte address for said word.

15. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode, the steps comprising:

switching from an active mode to a sleep mode;

identifying non-critical bit addresses;

encoding critical bits with an error correction code (ECC);

storing ECC codes in said non-critical bit addresses;

reducing a refresh rate for said memory;

performing error correction on said critical bits using said ECC codes when reentering active mode; and

discarding said ECC bits.

16. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

reducing said operating temperature by a 2X factor for each decade Celsius reduction in operating temperature.

17. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

preallocating addresses in memory to store non-critical bits.

18. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, the steps further comprising:

storing said ECC codes for a word of a last byte address for said word.

19. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15 wherein said error correction codes comprise Reed-Solomon code.

20. (Original) A computer readable medium embodying instructions for causing a computer to take steps to reduce the refresh rate of a memory in sleep mode as recited in claim 15, wherein said error correction codes comprise Bose-Chaudhuri-Hocquenghem code.

(9) EVIDENCE APPENDIX

None.

(10) RELATED PROCEEDINGS APPENDIX

None.